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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/538,684	03/30/00	KINSMAN	L 3056.1US (96

EXAMINER	
GRAYBILL,D	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 09/06/01

MM91/0906

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

1- File Copy

PTO-90C (Rev 2/95)

Office Action Summary	Application No. 09/538,684	Applicant(s) KINSMAN ET AL.	
	Examiner David E Graybill	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12,14-29,31-37 and 39-45* is/are pending in the application.

4a) Of the above claim(s) *7,21,23 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 6 8-12 14-20 22 24-29 31 33-37 39-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The amendment filed 6-19-01 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is the claims 2-4 and 27-29 limitation "a group consisting of." To further clarify, the limitation "a group consisting of" is an exclusive, negative limitation, and any exclusionary proviso or negative limitation must have basis in the original disclosure. See Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983) aff'd mem., 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation is not basis for an exclusion.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claims 2-4 and 27-29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The non-described subject matter is the claims 2-4 and 27-29 limitation "a group consisting of."

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 6, 8-12, 14-20, 22, 24-29, 31, 33-37 and 39-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 22, 24 and 25 there is insufficient literal antecedent basis for the term "the area of each of the plurality of leads."

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

Claims 1, 2, 4, 6, 8-12, 14-20, 24-27, 29, 31, 33-37 and 39-45 are rejected under 35 U.S.C. 102(b) as anticipated by

Marrs (5701034) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Marrs.

At column 1, lines 37-44; column 2, lines 33-42; column 3, lines 34-40; column 4, lines 6-16; column 5, lines 1-33; column 5, line 67 to column 6, line 23; column 6, lines 59-61; column 8, lines 63 and 64; column 10, lines 17, 18, 24 and 42-46; and column 11, lines 35 and 36, Marrs teaches the following:

1. An integrated circuit (IC) package comprising: a package body 120; an IC die 101 positioned within the package body; a lead frame including a plurality of leads 102 having portions enclosed within the package body that connect to the IC die; and an electrically conductive heat sink 110 positioned at least partially within the package body with a surface 110b of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink 110a projecting away from the first portion of the heat sink under the die-attach area and the IC die, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a

signal plane and a ground plane for the plurality of leads of the lead frame.

2. The IC package of claim 1, wherein the package body is selected from a group consisting of a transfer molded plastic package body and a preformed ceramic package body.

4. The IC package of claim 1, wherein the lead frame is selected from a group consisting of a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

6. The IC package of claim 1, wherein the heat sink is coupled to the reference voltage through one of a wirebond 117, a conductive adhesive, and a welded connection.

8. The IC package of claim 1, wherein the heat sink is positioned only partially within the package body (surface 110a is externally exposed).

9. The IC package of claim 1, wherein the heat sink is coupled to a printed circuit board outside the package body thereby coupled (by leads 102) to one of a signal voltage and a reference voltage.

10. The IC package of claim 8, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

11. The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

12. The IC package of claim 1, wherein the heat sink is positioned within the package body with its first portion extending i substantially to at least one side of the package body.

14. The IC package of claim 1, wherein the first and second portions of the heat sink are integral with one another.

15. The IC package of claim 1, wherein the first and second portions of the heat sink comprise separate parts.

16. The IC package of claim 1, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

17. The IC package of claim 1, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

18. The IC package of claim 1, wherein the heat sink has locking holes 112 therein for locking the heat sink in the IC package.

19. The IC package of claim 1, further comprising an adhesive 118 attaching the lead frame to the heat sink.

20. The IC package of claim 1, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

24. An integrated circuit (IC) package comprising: a package body; an IC die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion (rim/periphery/edge) having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area of the plurality of leads of the lead frame, the die-attach surface being attached to the IC die.

25. An integrated circuit (IC) package comprising: an IC die; a lead frame including a plurality of leads having portions that are connected to the IC die; and an electrically conductive heat sink positioned having a surface of a first portion of the heat

sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area and the IC die, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

26. The IC package of claim 25, further comprising a package body.

27. The IC package of claim 26, wherein the package body is selected from a group consisting of a transfer molded plastic package body and a preformed ceramic package body.

29. The IC package of claim 25, wherein the lead frame is selected from a group consisting of a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

31. The IC package of claim 25, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

33. The IC package of claim 26, wherein the heat sink is positioned only partially within the package body.

34. The IC package of claim 26, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

35. The IC package of claim 34, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

36. The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

37. The IC package of claim 26, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

39. The IC package of claim 25, wherein the first and second portions of the heat sink are integral with one another.

40. The IC package of claim 25, wherein the first and second portions of the heat sink comprise separate parts.

41. The IC package of claim 25, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

42. The IC package of claim 25, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

43. The IC package of claim 25, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

44. The IC package of claim 25, further comprising an adhesive attaching the lead frame to the heat sink.

45. The IC package of claim 25, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

To further clarify the teaching of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads, it is noted that it is inherent that the heat sink faces the lead frame in close proximity to a substantial part of the enclosed portion of 100 percent of the area of each of the plurality of leads that is attached to, and overlies the heat sink.

In any case, in the alternative, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular relative dimensions because applicant has not disclosed that the relative dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 3, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs as applied to claims 1, 2, 4-6, 8-20, 24-27, 29-31 and 33-45, and further in combination with Wark (5696031).

Marrs does not appear to explicitly teach the following:

3. The IC package of claim 1, wherein the IC die is selected from a group consisting of a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable ReadOnly Memory (EEPROM) IC die, and a processor IC die.

22. An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices including an integrated circuit (IC) package comprising: a package body; an IC die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area of each of the plurality of leads of the lead frame and having a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink being

opposite the die-attach area and projecting away from the first portion of the heat sink and the IC die.

28. The IC package of claim 25, wherein the IC die is selected from a group consisting of a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable ReadOnly Memory (EEPROM) IC die, and a processor IC die.

Nonetheless, at column 5, lines 59-65, Wark teaches these limitations. Moreover, it would have been obvious to combine the product of Wark with the product of Marrs because it would provide an electronic system.

Applicant's remarks filed 6-19-01 have been fully considered and are adequately addressed in the rejection supra.

Applicant's amendment necessitated the new grounds of rejection presented in this Office action.

In particular, in the previous Office action, the limitations in claims 11, 13, 36 and 38 directed to the heat sink proximity are definite and of different scope than the newly amendatory limitations directed to the heat sink proximity.

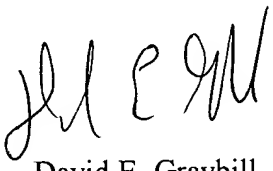
Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.



David E. Graybill
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Art Unit 2814

D.G.
5-Sep-01